L Lakshmanan

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Education

International Institute of Information Technology, Hyderabad, B.Tech. + M.S. by Research in Electronics and Communication Engineering — 2020 – 2025

- Advised by Dr. Aftab M. Hussain as part of the integrated Bachelor's and Master's by research program.
- GPA: 9.01/10.00
- **Coursework:** Advanced Computer Architecture, Introduction to Processor Architecture, Digital Systems and Microcontrollers, VLSI Design

Selected Research Experience

Visiting Research Student, School of Informatics, University of Edinburgh — July 2024 - Present

- Analysing the architectural bottlenecks for large serverless deployments, and contrasting them with the problems encountered with regular server workloads.
- Working on the vHive serverless ecosystem, analysing performance of serverless clusters with realistic functions from the vSwarm benchmark suite, improving the deployment framework for large loads.
- Advised by Dr. Boris Grot, in collaboration with Dr. David Schall.

Student Researcher, Centre for VLSI and Embedded Systems - IIIT Hyderabad — May 2022 - Present

- Working on research projects involving embedded systems, sensor networks, noise analysis, flexible electronics under the guidance of Dr. Aftab Hussain.
- Primarily worked on building low latency data collection systems which were used for collecting data towards driving data prediction tasks.

Student Researcher, Computer Systems Group, IIIT Hyderabad — Sept 2023 - Oct 2023

- Worked on deploying ML models on resource constrained embedded platforms for image recoginition tasks under the supervision of Dr. Suresh Purini.
- Helped develop an end-to-end pipeline for real-time image recognition using YOLOv5. Used the ONNX runtime and offloading computations to specialised accelerator cores, by which we achieved sustained performance of 90+ fps with object detection.

Research Collaborator, Remote, Polytechnic University of Catalonia — Jan 2024 - Oct 2024

- Worked on analysing GPU architectures for Ray-Tracing applications using Vulkan-sim and Lumibench under the guidance of Dr. Antonio Gonzalez.
- Identifying bottlenecks in the ray tracing pipeline that can potentially be solved by specific architectural modifications for SIMD and RT units as well as cache hierarchies.

Publications

* refers to equal contribution.

- **Lakshmanan, L.**, Hussain, A. (2024) Architecture of a Two-wheeler Mobile Sensing Platform for Riding Data Collection. **Accepted in IEEE ICVES 2024.**
- Goparaju, S., **Lakshmanan, L.**, Navnit, A., Rahul, B., Lovish, B., Gangadharan, D., Hussain, A. (2023) Time Series-based Driving Event Recognition for Two Wheelers. **Published in IEEE DATE 2023**.
- **Lakshmanan, L.***, Gupta, M.*, Fatema, A., Hussain, A. (2023) Characterisation and Quantification of Crosstalk on a Velostat-based Flexible Pressure Sensing Matrix. **Published in IEEE FLEPS 2023**.
- Gupta, M., **Lakshmanan, L.**, Fatema, A., Hussain, A. (2023) Flexible Writing Pad based on a Piezoresistive Thin Film Sensor Matrix. **Published in IEEE APSCON 2023.**

Professional Experience

Technical Program Manager Intern, Microsoft May 2024 - July 2024

- Worked with the Global Capacity Management team to plan, ideate and implement a new feature for the internal staffing tool.
- Feature aimed at improving the efficiency and ease of use for requestors by providing real-time feedback regarding request specifications and suggesting similar matches using a random forest regressor.

System Software Development Intern, Texas Instruments May 2023 - July 2023

- Ported AM62x SoC to **Zephyr Real Time Operating System** from the proprietary SDK, wrote driver for proprietary RAT **(Address Translation) module**
- Modified and improved open source drivers for UART and Pincontrol for supporting M4F core on the AM62x.
- All contributions can be found in the upstream repository: Zephyr RTOS

Open Source Developer, Free and Open Source Silicon (FOSSi) foundation, Google Summer of Code May 2022 - Sept 2022

- Worked on Sootty, the CLI waveform viewer.
- Improved the temporal logic language that Sootty uses by implementing bitwise operators for multi-wire busses, adding a save flag to allow for a reusable query interface.
- Added support for ready-valid handshake detection according to the AXI protocol.

Selected Projects

System Benchmark Suite

- Wrote a benchmark suite in C using vector intrinsics and some inline assembly to measure various aspects of performance of a computer system and its memory architecture, and to measure performance of various algorithms using cachegrind and perf.

Verilog Implementation of a 64-bit Y86 processor with Pipelining

- Constructed and tested two 64-bit processors with the Y86 instruction set architecture, one with sequential design and one with a full 5 stage pipeline. Tested functioning of all instructions for both. Used Verilog HDL. Project on Github.

Teaching Experience

Teaching Assistant, IIIT Hyderabad

- Scheduled tutorial sessions for students who take the Digital Systems and Microcontrollers course.
- Conducted hardware lab sessions and tutorials for over 300 students, headed a team of teaching assistants and evaluated coursework for two semesters.

Awards, Scholarships and Programmes

- **Undergraduate Research Award**: Award presented for exceptional research work in the year 2023.
- **Dean's List Award**: Award presented for exceptional academic performance in 4 semesters.
- **Andy Grove Scholarship**: Awarded by Intel for exceptional academic performance.
- **Winter School on Program Analysis and Optimization**: Selected to visit IIT Delhi and attend talks by researchers working on compilers, program analysis and optimization.